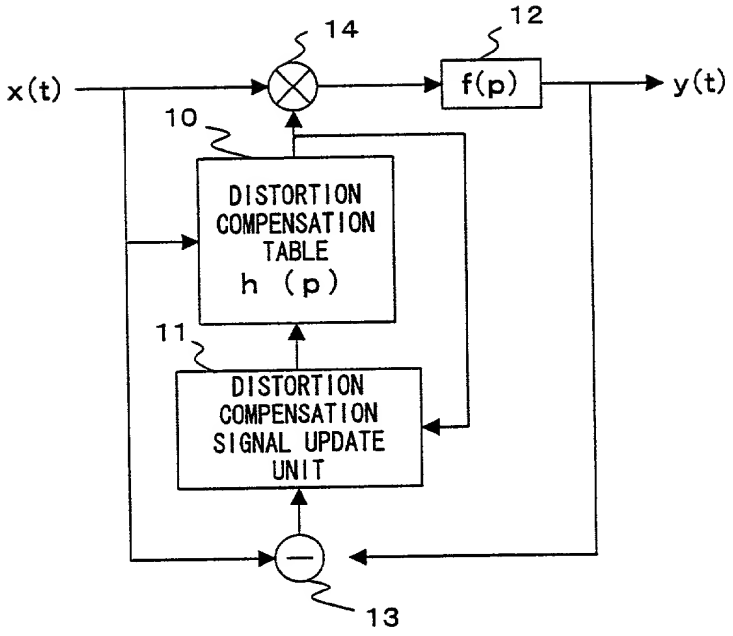

14
12
x(t)
f(p)
y(t)
10
DISTORTION
COMPENSATION
TABLE
h (p)
11
DISTORTION
COMPENSATION
SIGNAL UPDATE
UNIT
13

FIG. 1

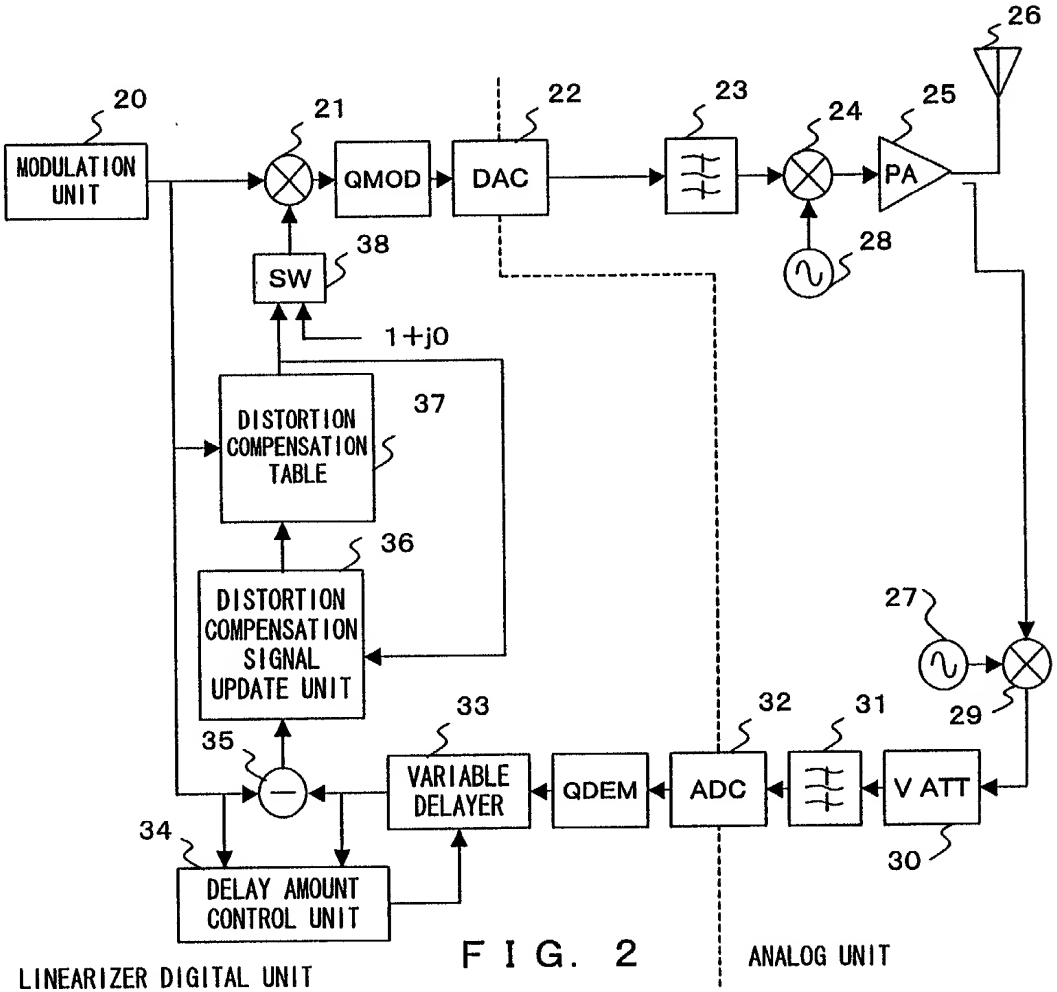


FIG. 2

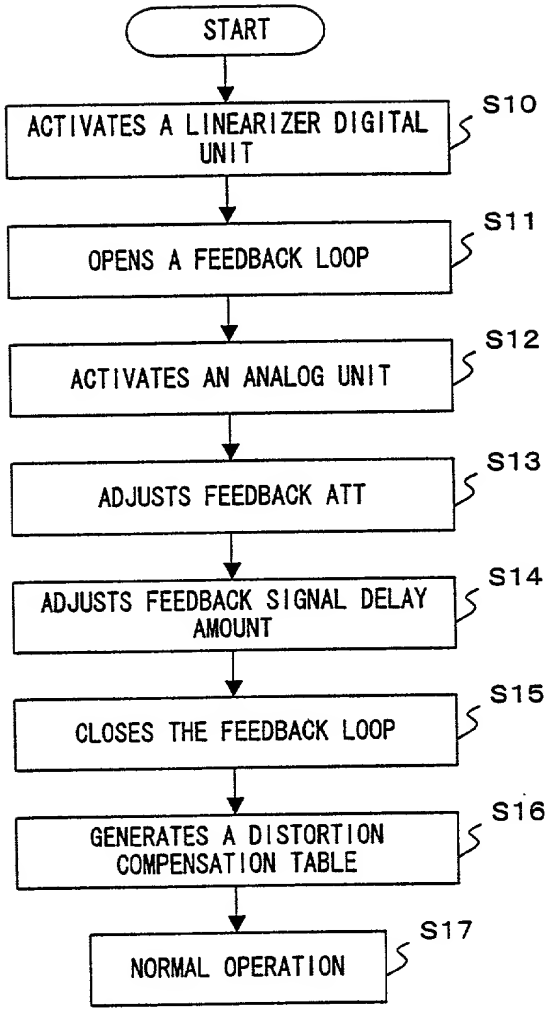
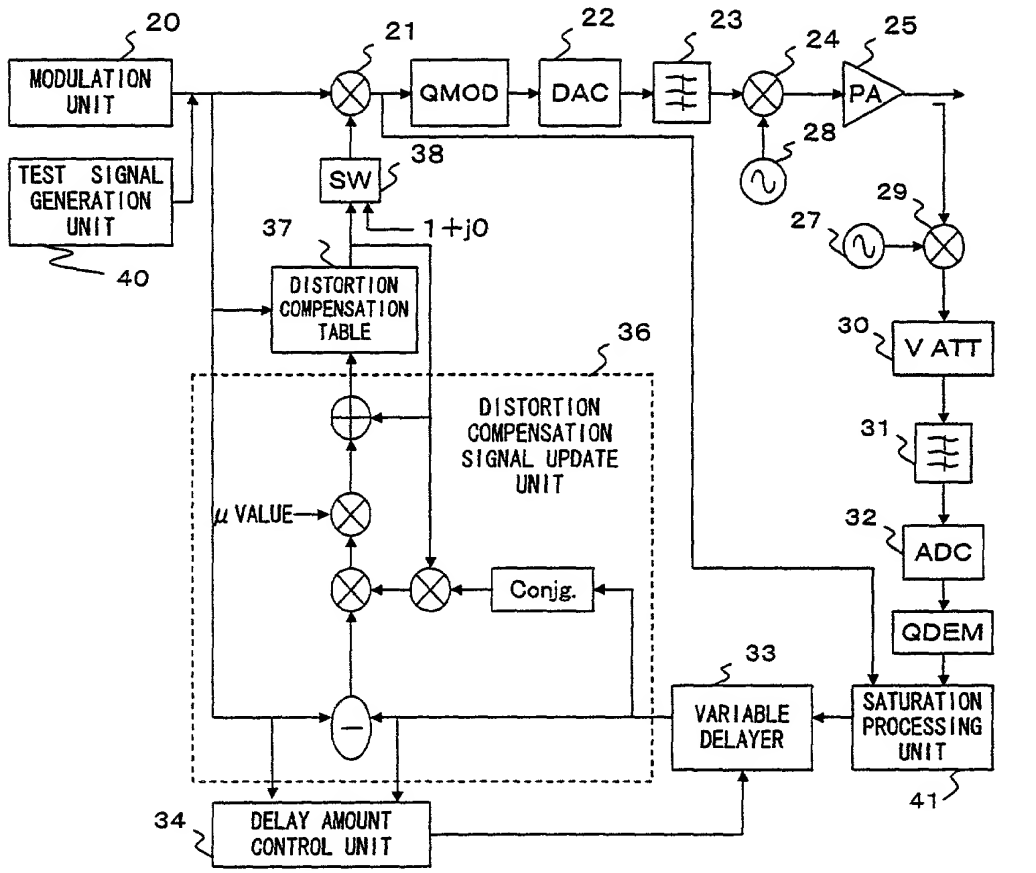
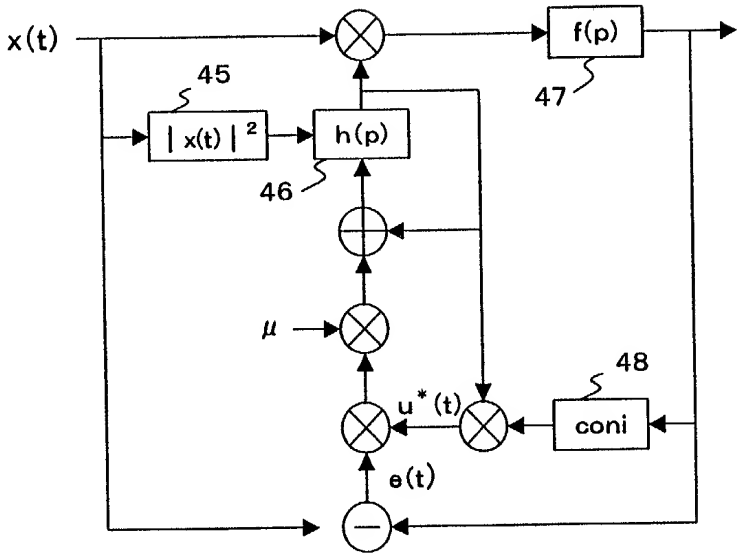

START
ACTIVATES A LINEARIZER DIGITAL UNIT
S10
OPENS A FEEDBACK LOOP
S11
ACTIVATES AN ANALOG UNIT
S12
ADJUSTS FEEDBACK ATT
S13
ADJUSTS FEEDBACK SIGNAL DELAY AMOUNT
S14
CLOSES THE FEEDBACK LOOP
S15
GENERATES A DISTORTION COMPENSATION TABLE
S16
NORMAL OPERATION
S17

FIG. 3



F I G. 4



$h_n(p)=h_{n-1}(p)+\mu\, e(t)u^*(t)$: LMSアルゴリズム
$e(t)=x(t)-y(t)$
$u(t)=x(t)f(p)\fallingdotseq h^*_{n-1}(p)y(t)$, $h_{n-1}(p)h^*_{n-1}(p)\fallingdotseq 1$
$y(t)=h_{n-1}(p)x(t)f(p)$
$p=|x(t)|^2$

x (t) : INPUT BAREBAND SIGNAL
f (p) : FUNCTION OF AMPLIFIER DISTORTION
h (p) : ESTIMATED DISTORTION COMPENSATION COEFFICIENT (COMPENSATION TABLE)
μ : STEP SIZE ϕ PARAMETER

FIG. 5

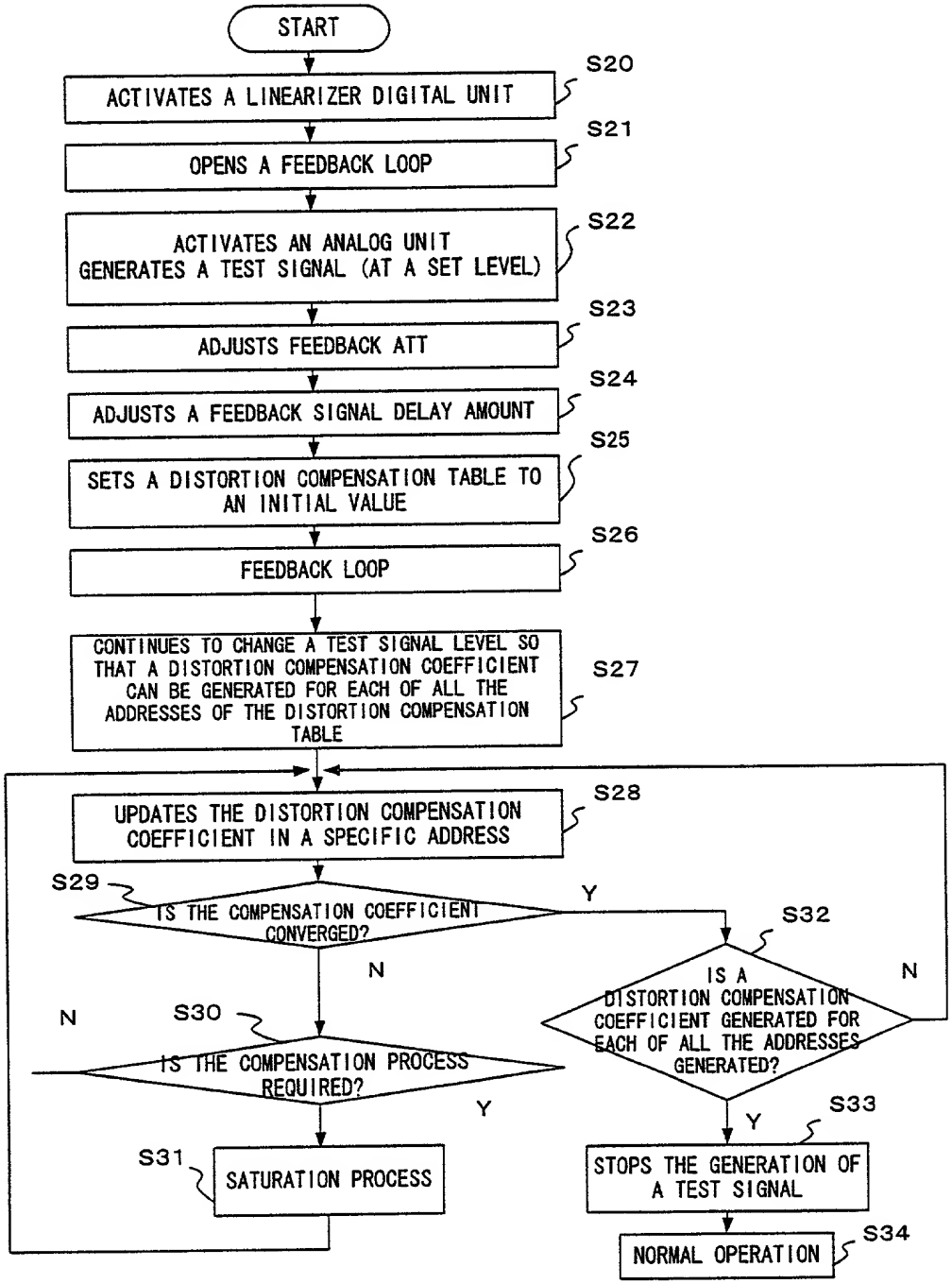
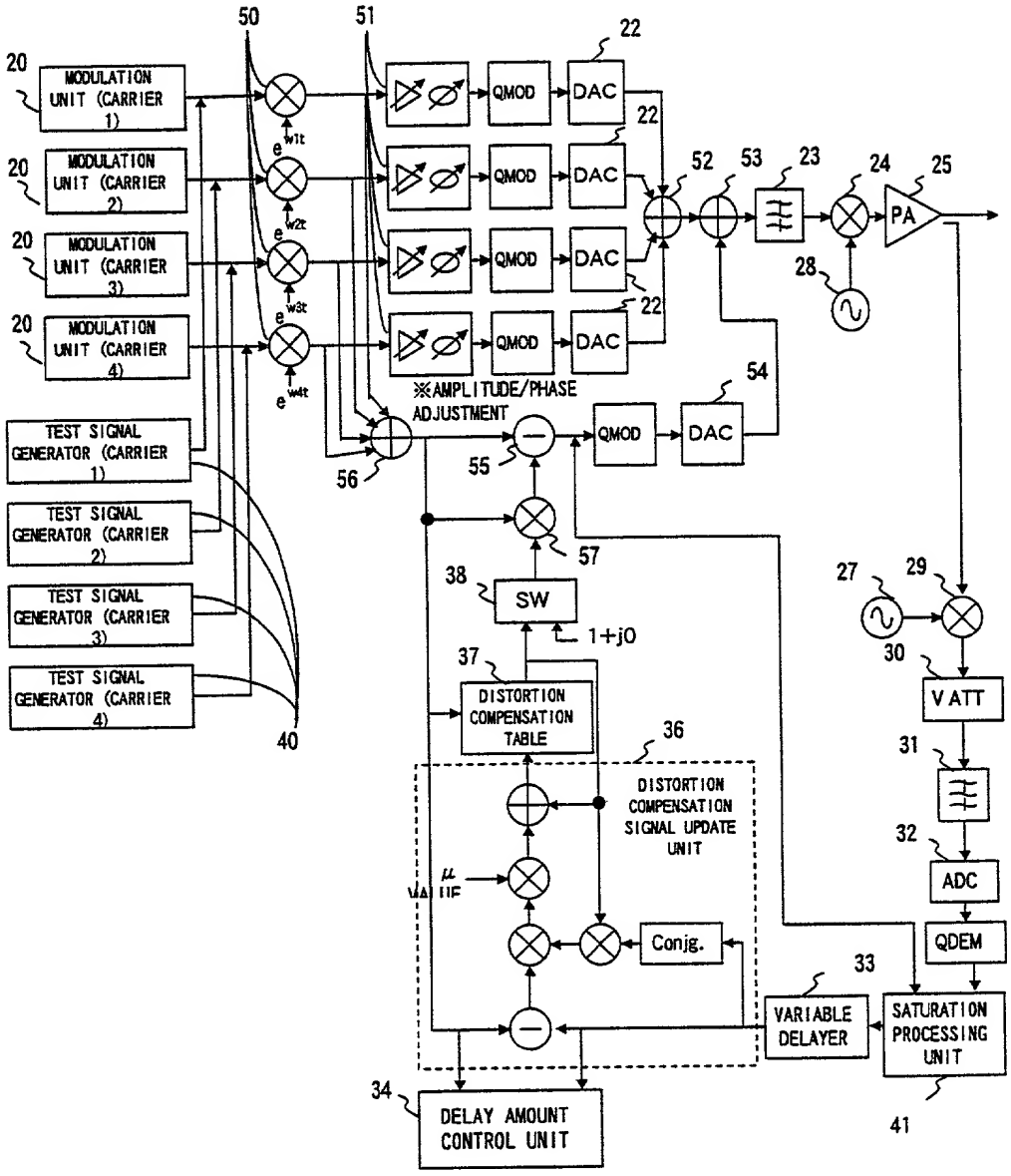

START
S20
ACTIVATES A LINEARIZER DIGITAL UNIT
S21
OPENS A FEEDBACK LOOP
S22
ACTIVATES AN ANALOG UNIT
GENERATES A TEST SIGNAL (AT A SET LEVEL)
S23
ADJUSTS FEEDBACK ATT
S24
ADJUSTS A FEEDBACK SIGNAL DELAY AMOUNT
S25
SETS A DISTORTION COMPENSATION TABLE TO AN INITIAL VALUE
S26
FEEDBACK LOOP
S27
CONTINUES TO CHANGE A TEST SIGNAL LEVEL SO THAT A DISTORTION COMPENSATION COEFFICIENT CAN BE GENERATED FOR EACH OF ALL THE ADDRESSES OF THE DISTORTION COMPENSATION TABLE
S28
UPDATES THE DISTORTION COMPENSATION COEFFICIENT IN A SPECIFIC ADDRESS
S29
IS THE COMPENSATION COEFFICIENT CONVERGED?
Y
N
S32
IS A DISTORTION COMPENSATION COEFFICIENT GENERATED FOR EACH OF ALL THE ADDRESSES GENERATED?
N
Y
S30
IS THE COMPENSATION PROCESS REQUIRED?
N
Y
S31
SATURATION PROCESS
S33
STOPS THE GENERATION OF A TEST SIGNAL
S34
NORMAL OPERATION

FIG. 6


MODULATION UNIT (CARRIER 1)
MODULATION UNIT (CARRIER 2)
MODULATION UNIT (CARRIER 3)
MODULATION UNIT (CARRIER 4)
TEST SIGNAL GENERATOR (CARRIER 1)
TEST SIGNAL GENERATOR (CARRIER 2)
TEST SIGNAL GENERATOR (CARRIER 3)
TEST SIGNAL GENERATOR (CARRIER 4)
QMOD
DAC
※AMPLITUDE/PHASE ADJUSTMENT
SW
1+j0
DISTORTION COMPENSATION TABLE
DISTORTION COMPENSATION SIGNAL UPDATE UNIT
Conjg.
DELAY AMOUNT CONTROL UNIT
VARIABLE DELAYER
SATURATION PROCESSING UNIT
PA
VATT
ADC
QDEM

F I G. 7

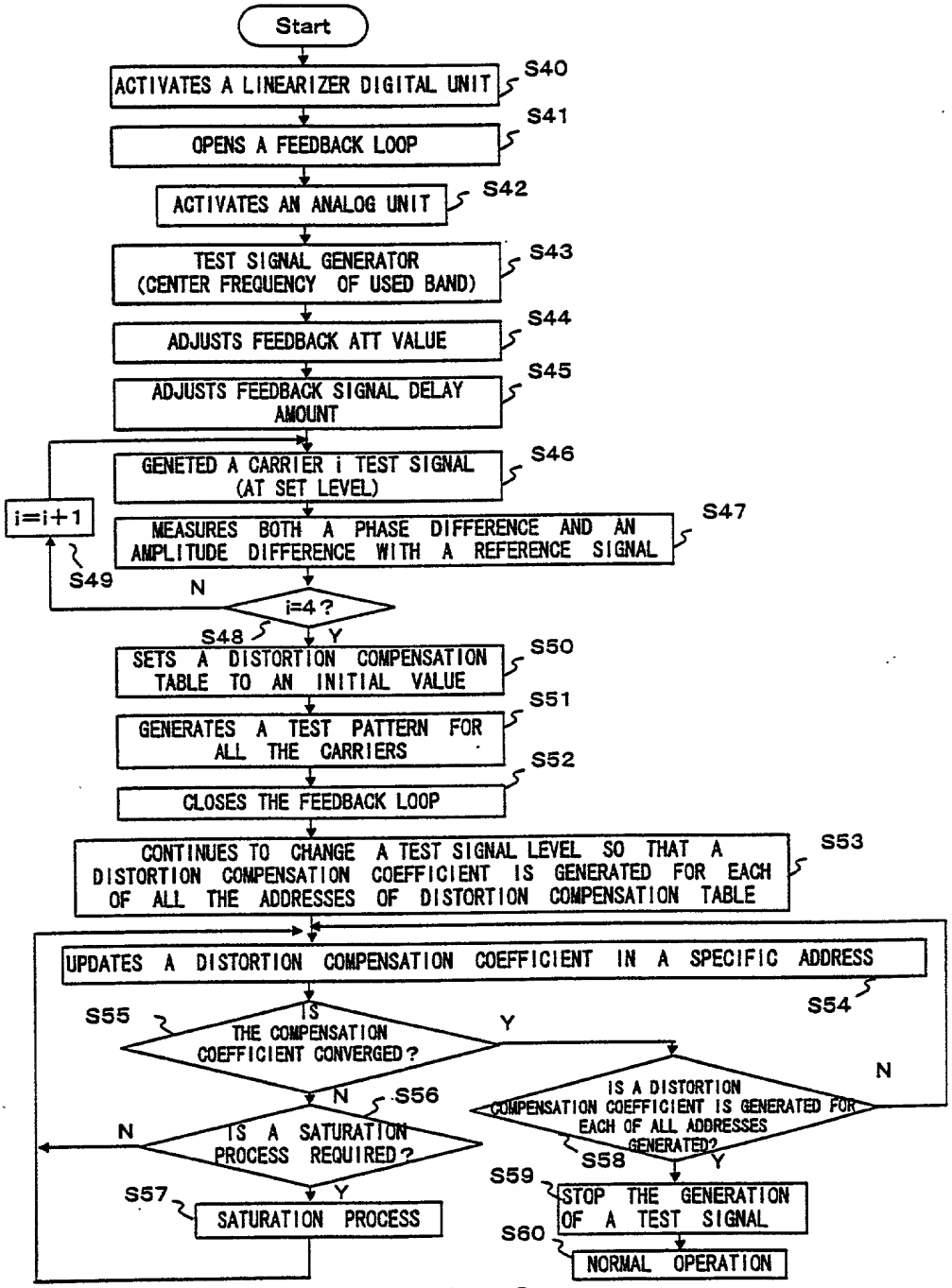

Start
ACTIVATES A LINEARIZER DIGITAL UNIT
S40
OPENS A FEEDBACK LOOP
S41
ACTIVATES AN ANALOG UNIT
S42
TEST SIGNAL GENERATOR (CENTER FREQUENCY OF USED BAND)
S43
ADJUSTS FEEDBACK ATT VALUE
S44
ADJUSTS FEEDBACK SIGNAL DELAY AMOUNT
S45
GENETED A CARRIER i TEST SIGNAL (AT SET LEVEL)
S46
MEASURES BOTH A PHASE DIFFERENCE AND AN AMPLITUDE DIFFERENCE WITH A REFERENCE SIGNAL
S47
i=i+1
S49
N
i=4?
S48
Y
SETS A DISTORTION COMPENSATION TABLE TO AN INITIAL VALUE
S50
GENERATES A TEST PATTERN FOR ALL THE CARRIERS
S51
CLOSES THE FEEDBACK LOOP
S52
CONTINUES TO CHANGE A TEST SIGNAL LEVEL SO THAT A DISTORTION COMPENSATION COEFFICIENT IS GENERATED FOR EACH OF ALL THE ADDRESSES OF DISTORTION COMPENSATION TABLE
S53
UPDATES A DISTORTION COMPENSATION COEFFICIENT IN A SPECIFIC ADDRESS
S54
S55
IS THE COMPENSATION COEFFICIENT CONVERGED?
Y
N
S56
IS A SATURATION PROCESS REQUIRED?
N
Y
S57
SATURATION PROCESS
IS A DISTORTION COMPENSATION COEFFICIENT IS GENERATED FOR EACH OF ALL ADDRESSES GENERATED?
N
S58
Y
S59
STOP THE GENERATION OF A TEST SIGNAL
S60
NORMAL OPERATION

FIG. 8

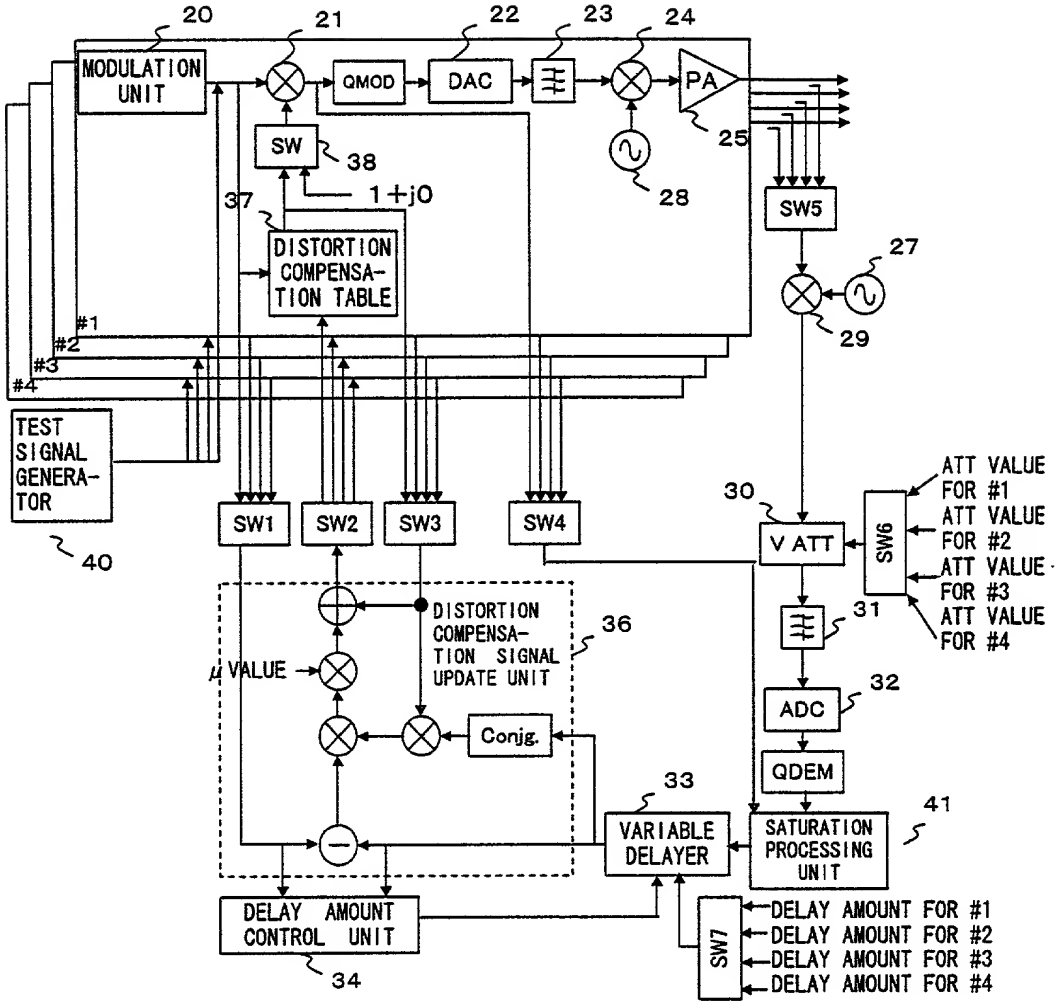

20
21
22
23
24
MODULATION UNIT
QMOD
DAC
PA
25
SW
38
1+j0
37
28
DISTORTION COMPENSATION TABLE
SW5
27
29
#1
#2
#3
#4
TEST SIGNAL GENERATOR
40
SW1
SW2
SW3
SW4
30
V ATT
SW6
ATT VALUE FOR #1
ATT VALUE FOR #2
ATT VALUE FOR #3
ATT VALUE FOR #4
31
32
ADC
QDEM
μ VALUE
DISTORTION COMPENSATION SIGNAL UPDATE UNIT
36
Conjg.
33
VARIABLE DELAYER
SATURATION PROCESSING UNIT
41
DELAY AMOUNT CONTROL UNIT
34
SW7
DELAY AMOUNT FOR #1
DELAY AMOUNT FOR #2
DELAY AMOUNT FOR #3
DELAY AMOUNT FOR #4

FIG. 9

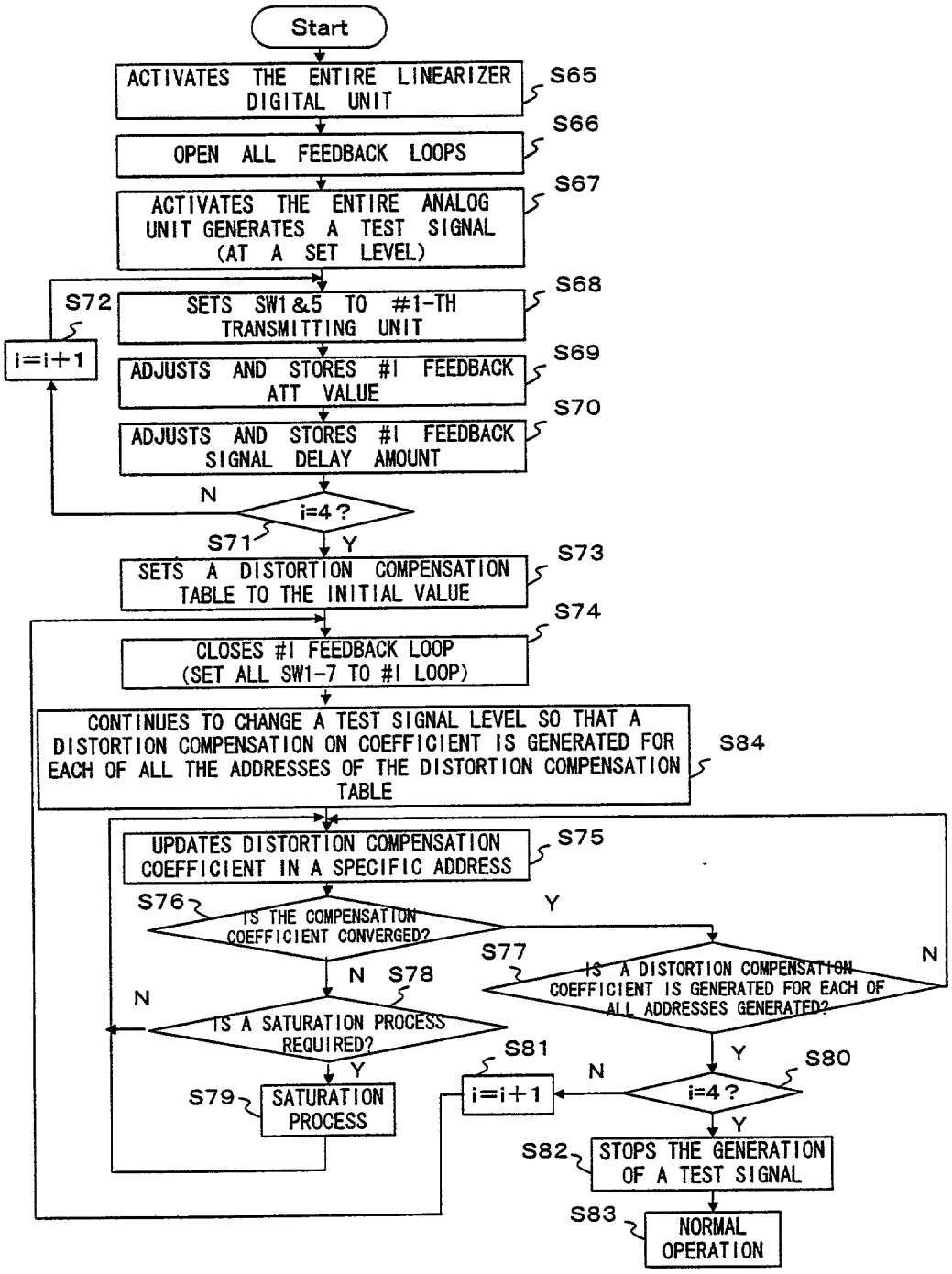

Start
ACTIVATES THE ENTIRE LINEARIZER DIGITAL UNIT
S65
OPEN ALL FEEDBACK LOOPS
S66
ACTIVATES THE ENTIRE ANALOG UNIT GENERATES A TEST SIGNAL (AT A SET LEVEL)
S67
SETS SW1&5 TO #1-TH TRANSMITTING UNIT
S68
ADJUSTS AND STORES #I FEEDBACK ATT VALUE
S69
ADJUSTS AND STORES #I FEEDBACK SIGNAL DELAY AMOUNT
S70
i=4?
N
Y
S71
i=i+1
S72
SETS A DISTORTION COMPENSATION TABLE TO THE INITIAL VALUE
S73
CLOSES #I FEEDBACK LOOP (SET ALL SW1-7 TO #I LOOP)
S74
CONTINUES TO CHANGE A TEST SIGNAL LEVEL SO THAT A DISTORTION COMPENSATION ON COEFFICIENT IS GENERATED FOR EACH OF ALL THE ADDRESSES OF THE DISTORTION COMPENSATION TABLE
S84
UPDATES DISTORTION COMPENSATION COEFFICIENT IN A SPECIFIC ADDRESS
S75
IS THE COMPENSATION COEFFICIENT CONVERGED?
S76
Y
N
IS A SATURATION PROCESS REQUIRED?
S78
N
Y
SATURATION PROCESS
S79
IS A DISTORTION COMPENSATION COEFFICIENT IS GENERATED FOR EACH OF ALL ADDRESSES GENERATED?
S77
N
Y
i=4?
S80
N
Y
i=i+1
S81
STOPS THE GENERATION OF A TEST SIGNAL
S82
NORMAL OPERATION
S83

FIG. 10

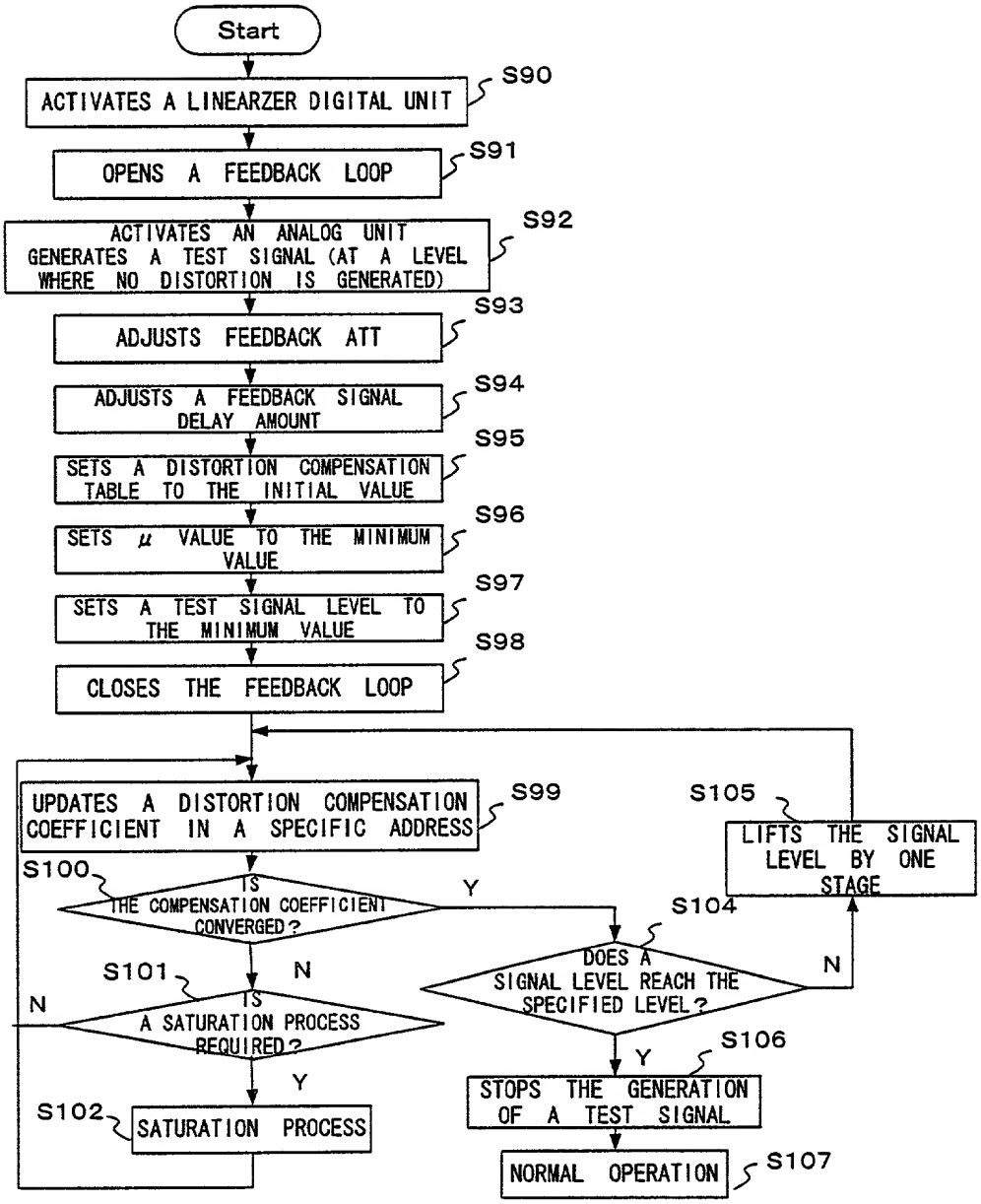

Start
ACTIVATES A LINEARZER DIGITAL UNIT
S90
OPENS A FEEDBACK LOOP
S91
ACTIVATES AN ANALOG UNIT GENERATES A TEST SIGNAL (AT A LEVEL WHERE NO DISTORTION IS GENERATED)
S92
ADJUSTS FEEDBACK ATT
S93
ADJUSTS A FEEDBACK SIGNAL DELAY AMOUNT
S94
SETS A DISTORTION COMPENSATION TABLE TO THE INITIAL VALUE
S95
SETS μ VALUE TO THE MINIMUM VALUE
S96
SETS A TEST SIGNAL LEVEL TO THE MINIMUM VALUE
S97
CLOSES THE FEEDBACK LOOP
S98
UPDATES A DISTORTION COMPENSATION COEFFICIENT IN A SPECIFIC ADDRESS
S99
S100
IS THE COMPENSATION COEFFICIENT CONVERGED?
Y
N
S101
IS A SATURATION PROCESS REQUIRED?
N
Y
S102
SATURATION PROCESS
S104
DOES A SIGNAL LEVEL REACH THE SPECIFIED LEVEL?
N
Y
S105
LIFTS THE SIGNAL LEVEL BY ONE STAGE
S106
STOPS THE GENERATION OF A TEST SIGNAL
NORMAL OPERATION
S107

FIG. 11

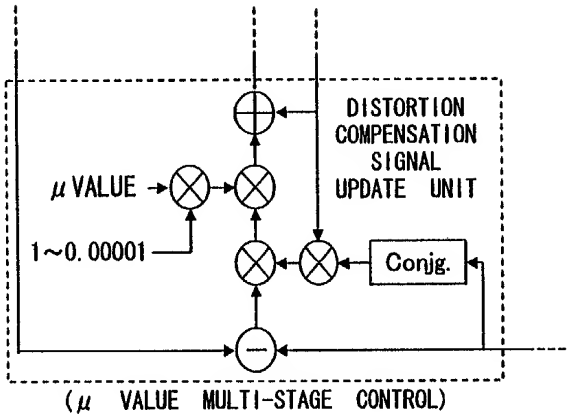


FIG. 12A

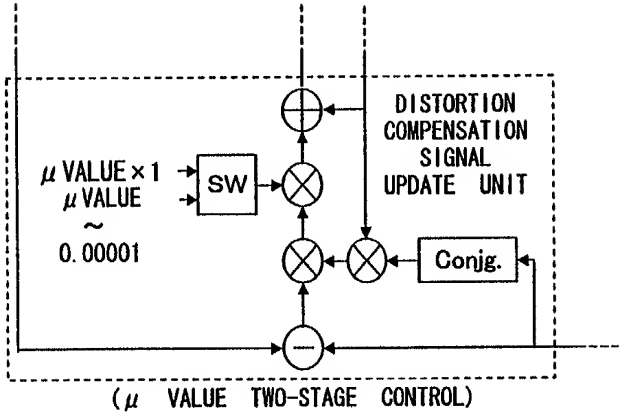


FIG. 12B

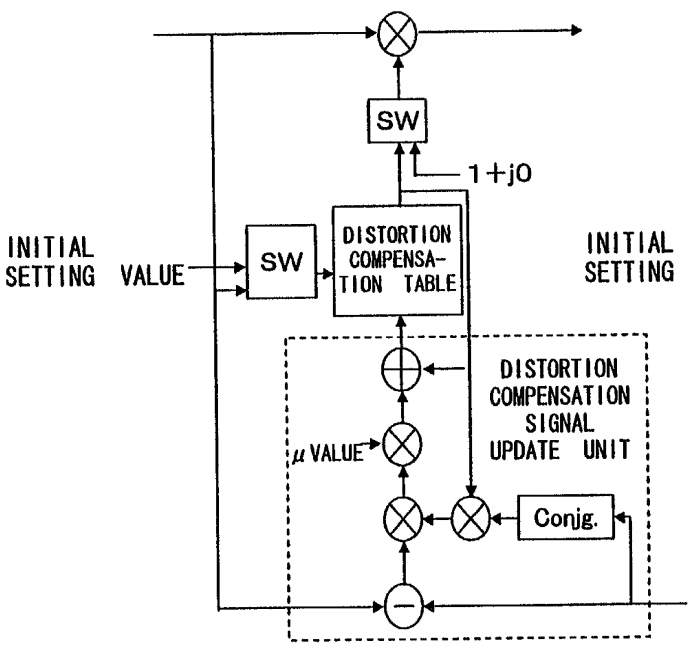


FIG. 13A

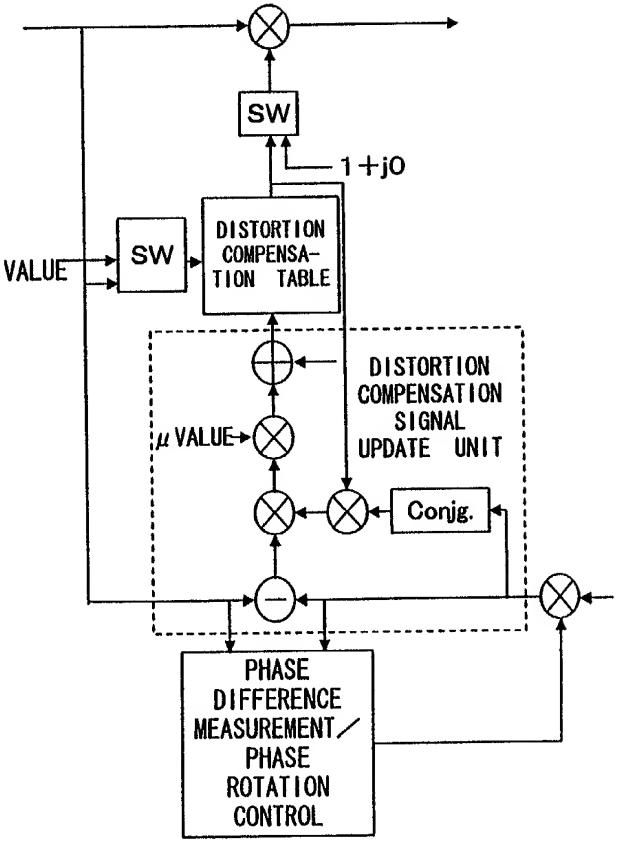


FIG. 13B

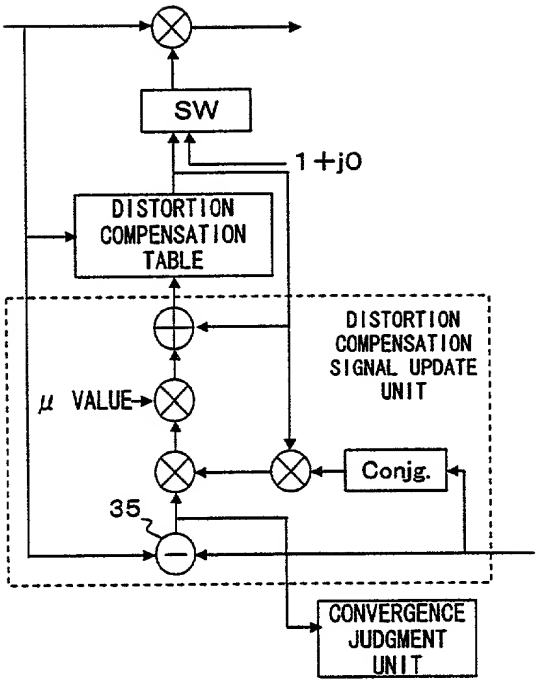

SW
1+j0
DISTORTION COMPENSATION TABLE
DISTORTION COMPENSATION SIGNAL UPDATE UNIT
μ VALUE
Conjg.
35
CONVERGENCE JUDGMENT UNIT

FIG. 14

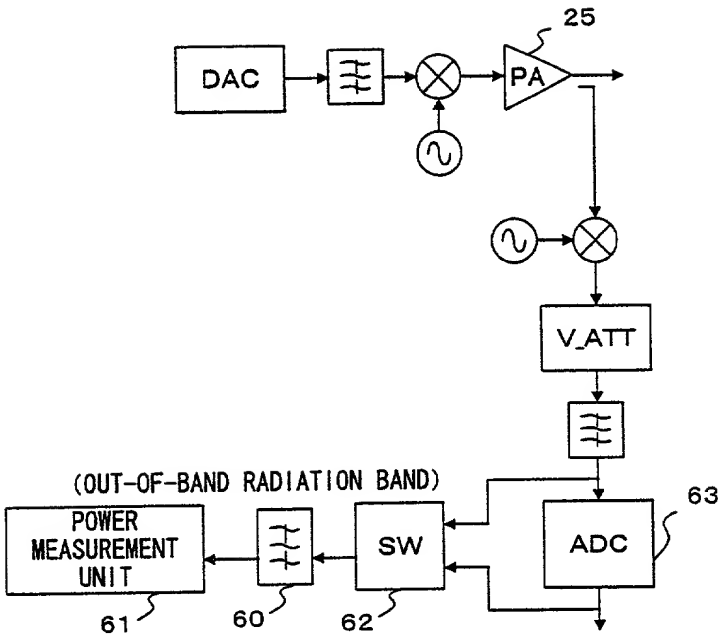

25
DAC
PA
V_ATT
(OUT-OF-BAND RADIATION BAND)
POWER MEASUREMENT UNIT
SW
ADC
63
61
60
62

FIG. 15

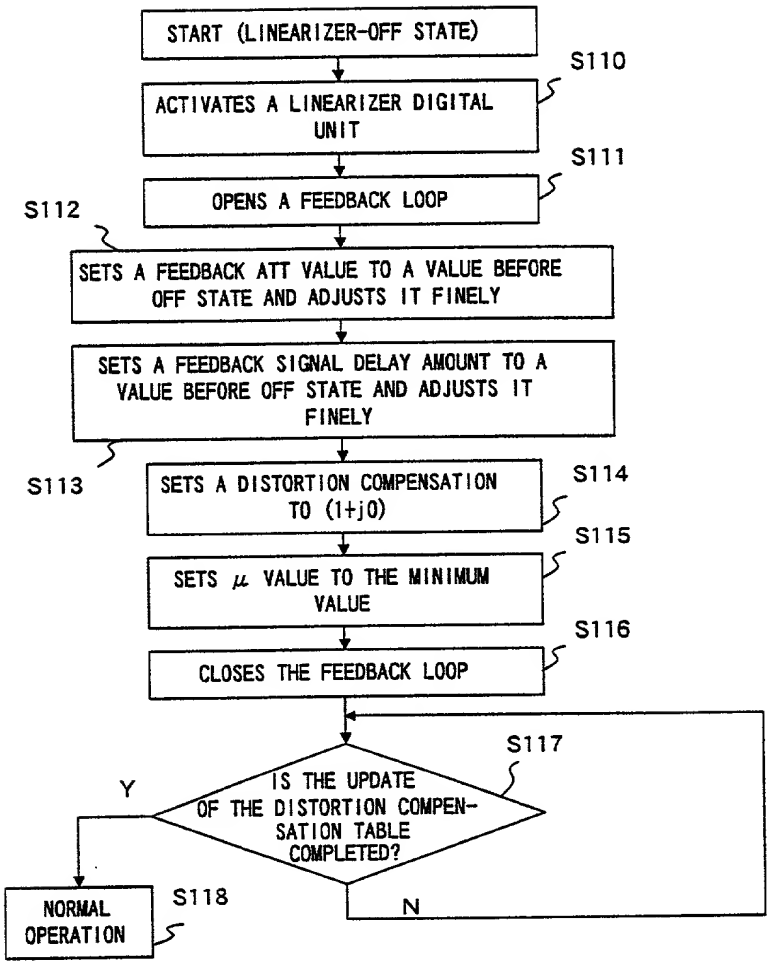

START (LINEARIZER-OFF STATE)
S110
ACTIVATES A LINEARIZER DIGITAL UNIT
S111
OPENS A FEEDBACK LOOP
S112
SETS A FEEDBACK ATT VALUE TO A VALUE BEFORE OFF STATE AND ADJUSTS IT FINELY
SETS A FEEDBACK SIGNAL DELAY AMOUNT TO A VALUE BEFORE OFF STATE AND ADJUSTS IT FINELY
S113
SETS A DISTORTION COMPENSATION TO (1+j0)
S114
SETS μ VALUE TO THE MINIMUM VALUE
S115
CLOSES THE FEEDBACK LOOP
S116
S117
IS THE UPDATE OF THE DISTORTION COMPEN-SATION TABLE COMPLETED?
Y
N
NORMAL OPERATION
S118

FIG. 16

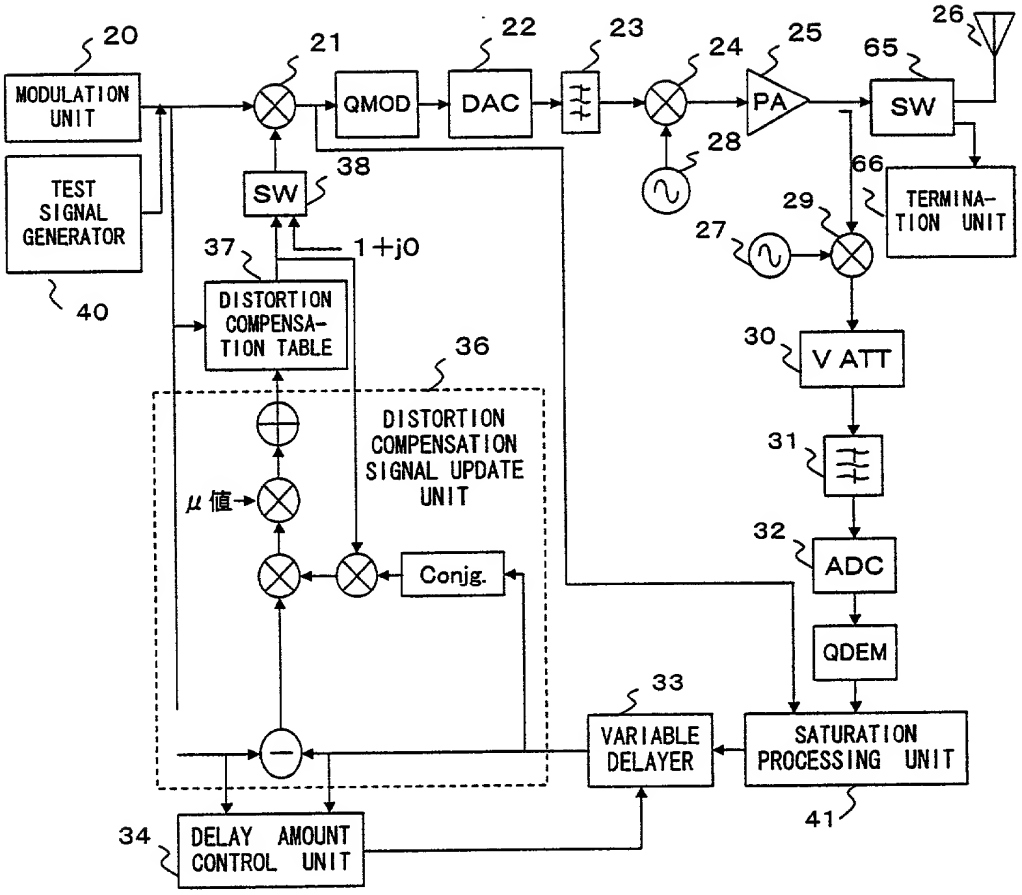

20
MODULATION UNIT
TEST SIGNAL GENERATOR
40
21
QMOD
22
DAC
23
24
25
PA
26
65
SW
66
TERMINA-TION UNIT
28
29
27
38
SW
1+j0
37
DISTORTION COMPENSA-TION TABLE
36
DISTORTION COMPENSATION SIGNAL UPDATE UNIT
μ値
Conjg.
30
V ATT
31
32
ADC
QDEM
33
VARIABLE DELAYER
SATURATION PROCESSING UNIT
41
34
DELAY AMOUNT CONTROL UNIT

FIG. 17